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EXAMINER	
STOYNOV, STEFAN	

ART UNIT	PAPER NUMBER
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/684,789	NOVAK ET AL.	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10,12-18,20-25,27,29,30 and 32* is/are rejected.

7)☒ Claim(s) *3,11,19,26,28 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

Claims 19 and 27 are objected to because of the following informalities:

The dependency for claim 19 appears to be mistaken. For the purpose of examination claim 19 is considered being dependent on claim 18.

Claim 27 recites the limitation "the at least one data processor" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-6, 8-10, 12, 13, 15-18, 20, 21, and 23-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Yanagawa, U.S. Patent Appl. Pub. No. 2001/0046163.

Re claims 1 and 17, Yanagawa discloses a data memory interface apparatus and a method of interfacing to a data memory comprising:

at least one interface for transmitting data and receiving data at a first data rate (paragraph 0045, lines 1-9, FIG. 1, 10, 12);

at least one memory interface for transmitting data to and receiving data from at least one dual data rate memory at a second rate (paragraph 0045, lines 1-6, lines 9-11, FIG. 1, 10, 11, paragraph 0002, lines 4-8);

at least one processing circuit for generating and receiving at least one dual edged data strobe to transmit data and to receive data from the at least one dual data rate memory (paragraph 0047, lines 1-8, FIG. 1).

[Yanagawa discloses the memory controller being an intermediary for control between the microprocessor and the dual data rate memory (paragraph 0045, lines 1-6). In addition, Yanagawa discloses the processor interfacing with the memory controller via a 64-bit wide bus and further the memory controller being connected with the dual data rate memory via a 32-bit wide bus (FIG. 2, DATA (64bit) and DATA (32bit)). To take advantage of the dual data rate memory, the data stored in separate latches within the memory controller (each holding 32 bits) is alternatively transferred on the rising and falling edges of the strobe signal (as described above) and implementing a higher clock frequency (paragraph 0051, line 1 – paragraph 0053, line 14). Thus, on one side of the memory controller (towards the processor) the transmission and reception of data is based on first data rate, whereas the transmission and reception of data on the other side of the memory controller (towards the dual data rate memory) is based on a second data rate. Thus, Yanagawa inherently discloses at least one interface for transmitting data and receiving data at a first data rate and at least one memory interface for transmitting data to and receiving data from at least one dual data rate memory at a second rate].

Re claims 2 and 18, Yanagawa further discloses the apparatus and method wherein the at least one interface uses a clock operating at the second frequency data rate and at least one phase reference signal to clock data into or out of the at least one

interface (paragraph 0053, lines 1-9, paragraph 0054, lines 1-6, paragraph 0056, lines 1-3, paragraph 0058, lines 1-6, paragraph 0059, lines 1-3).

Re claims 4 and 20, Yanagawa further discloses the apparatus and method as per claims 2 and 18 wherein the at least one phase reference signal is distributed in a daisy chain to a plurality of processing modules in the at least one of processing circuit (paragraph 0054 lines 1-6, paragraph 0056, lines 1-11, FIG. 3, 51-1 – 51-4).

Re claim 5, Yanagawa further discloses the apparatus wherein the at least one interface comprises at least one register for clocking data into or out of the at least one interface according to a clock operating at the second data rate (paragraph 0051, line 1 – paragraph 0053, line 14, FIG. 2).

Re claims 6 and 21, Yanagawa further discloses the apparatus and method wherein the at least one processing circuit comprises at least one delay lock loop for delaying the at least one dual-edged data strobe (paragraph 0063, lines 1-9, paragraph 0065, lines 1-5, paragraph 0085, lines 1-10, FIG. 5, 6, and 7).

Re claims 8 and 23, Yanagawa further discloses the apparatus and method wherein the at least one processing circuit comprises at least one alternating inverting tree for generating the at least one dual-edged data strobe (paragraph 0122, lines 1-8, FIG. 14).

Re claims 9 and 24, Yanagawa further discloses the apparatus and method wherein the at least one processing circuit generates data according to a first edge of a clock operating at the second data rate and generates the at least one dual-edged data

strobe according to a second edge of the clock that immediately follows the first edge (paragraph 0121, lines 12-19, FIG. 13B).

Re claims 10 and 25, Yanagawa further discloses the apparatus and method wherein the at least one processing circuit selectively gates the at least one dual-edged data strobe when receiving data from the at least one dual data rate memory (paragraph 0053, lines 1-14, paragraph 0058, lines 1-6, paragraph 0065, line 1 – paragraph 0072, line 4).

Re claim 12, Yanagawa further discloses the apparatus wherein the at least one processing circuit comprises a plurality of processing modules for processing bytes of data transmitted to and received from the at least one dual data rate memory (FIG. 2, processing modules in 10).

Re claim 13, Yanagawa further discloses the apparatus wherein the at least one processing circuit comprises at least one data memory for storing data received from the at least one dual data rate memory (FIG. 2, LATCH CIRCUIT 27, 32, 33).

Re claim 15, Yanagawa further discloses the apparatus wherein the at least one dual data rate memory comprises DDR SDRAM (paragraph 0113, lines 1-19).

Re claim 16, Yanagawa further discloses the apparatus wherein the at least one interface comprises at least one buffer (FIG. 2, LATCH CIRCUIT 27, 32, 33).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 7 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagawa U.S. Patent Appl. Pub. No. 2001/0046163.

Re claims 7 and 22, Yanagawa discloses the apparatus and method as per claims 6 and 21.

Yanagawa does not specifically state the at least one delay lock loop provides substantially equal delays for a 100 MHz dual-edged data strobe and a 133 MHz dual-edged data strobe. However Yanagawa discloses plurality of variable delay elements (included in the delay locked loop as described previously) (FIG. 3, 51-1 – 51-5) where each variable delay element provides a variable and equal delay for the strobe signal (paragraph 0062, lines 1-10). Thus, the delay affecting the strobe signal is variable (applicable for different strobe clock frequencies e.g. 100 MHz and 130 MHz) for accommodating different data rates. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use variable delay lock loop providing variable delays for the data strobe signal, as suggested by Yanagawa in order to implement the at least one delay lock loop provides substantially equal delays for a

100 MHz dual-edged data strobe and a 133 MHz dual-edged data strobe. One of ordinary skill in the art would be motivated to do so in order to accommodate the different dual data rate memories operating at different clock frequencies.

Claims 14, 27, 29, 30, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagawa U.S. Patent Appl. Pub. No. 2001/0046163 in view of Lai et al., U.S. Patent No. 6,738,880.

Re claim 14, Yanagawa discloses the apparatus as per claim 13.

Re claim 27, Yanagawa discloses a data memory interface apparatus comprising:

at least one interface for transmitting data to and receiving data from at least one data processor at a first data rate using a clock signal operating at a second data rate and a phase reference signal (paragraph 0045, lines 1-9, FIG. 1, 10, 12, paragraph 0051, lines 1-12, paragraph 0053, lines 1-9, paragraph 0054, lines 1-6, paragraph 0056, lines 1-3, paragraph 0058, lines 1-6, paragraph 0059, lines 1-3);

[Yanagawa discloses the memory controller being an intermediary for control between the microprocessor and the dual data rate memory (paragraph 0045, lines 1-6). In addition, Yanagawa discloses the processor interfacing with the memory controller via a 64-bit wide bus and further the memory controller being connected with the dual data rate memory via a 32-bit wide bus (FIG. 2, DATA (64bit) and DATA (32bit)). To take advantage of the dual data rate memory, the data stored in separate latches within the memory controller (each holding 32 bits) is alternatively transferred on the rising and falling edges of the strobe signal (as described above) and implementing a higher clock

frequency (paragraph 0051, line 1 – paragraph 0053, line 14). Thus, on one side of the memory controller (towards the processor) the transmission and reception of data is based on first data rate, whereas the transmission and reception of data on the other side of the memory controller (towards the dual data rate memory) is based on a second data rate. Thus, Yanagawa inherently discloses at least one interface for transmitting data to and receiving data from at least one data processor at a first data rate using a clock signal operating at a second data rate and a phase reference signal (the reference signal addressed above)].

at least one memory interface for transmitting data to and receiving data from at least one DDR SDRAM at a second data rate according to at least one DQS signal (paragraph 0047, lines 1-8, FIG. 1, paragraph 0113, lines 1-19);

at least one processing circuit comprising:

at least one circuit for selectively gating at least one DQS signal received from the at least one DDR SDRAM (paragraph 0053, lines 1-14, paragraph 0058, lines 1-6, paragraph 0065, line 1 – paragraph 0072, line 4);

at least one delay lock loop for delaying at least one DQS signal received from the at least one DDR SDRAM (paragraph 0063, lines 1-9, paragraph 0065, lines 1-5, paragraph 0085, lines 1-10, FIG. 5, 6, and 7); and

and at least one alternating inverting buffer tree for generating a plurality of DQS signals from the delayed at least one DQS signal to clock data (paragraph 0122, lines 1-8, FIG. 14).

Re claim 14, Yanagawa fails to disclose the at least one data memory comprises at least one FIFO.

Re claim 27, Yanagawa fails to disclose at least one FIFO for storing data received from the at least one DDR SDRAM and clock data into the at least one FIFO.

Lai teaches a buffer in a memory access system (column 1, lines 14-15) including two FIFO buffer memories for buffering the data transferred between the memory and the control chip set (column 2, lines 13-19, FIG. 3, 342, 344). In Lai, the memory buffer is used with DDR DRAM memory (column 1, lines 26-26) and provides for interfacing between the slower memory and faster processor (column 1, lines 36-40. Thus, the necessity for lowering the processor's speed in order to accommodate the slower memory data transfer is avoided (column 1, lines 49-53).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the memory interface buffer including FIFO memories, as suggested by Lai with the apparatus disclosed by Yanagawa in order to implement the at least one data memory comprises at least one FIFO, at least one FIFO for storing data received from the at least one DDR SDRAM, and clock data into the at least one FIFO. One of ordinary skill in the art would be motivated to do so in order to prevent from lowering the fast processor clock when operating with lower data transfer memory.

Re claim 29, Yanagawa further discloses the apparatus wherein the at least one phase reference signal is distributed in a daisy chain to a plurality of processing modules in the at least one processing circuit (paragraph 0054 lines 1-6, paragraph 0056, lines 1-11, FIG. 3, 51-1 – 51-4).

Re claim 30, Yanagawa further discloses the apparatus, wherein the at least one processing circuit generates data according to a first edge of a clock operating at the second data rate and generates the at least one DQS signal according to a second edge of the clock that immediately follows the first edge (paragraph 0121, lines 12-19, FIG. 13B).

Re claim 32, Yanagawa further discloses the apparatus wherein the at least one processing circuit comprises a plurality of processing modules for processing bytes of data transmitted to and received from the at least one DDR SDRAM (FIG. 2, processing modules in 10).

Allowable Subject Matter

Claims 3, 11, 19, 26, 28, and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Re claims 3, 19, and 28, the prior art of record fails to discloses or suggest, individually or in combination the apparatus and method as per claims 2, 18, and 27 wherein "the at least one phase reference signal is indicative of either rising edges or falling edges of a clock operating at the first data rate".

Re claims 11, 26, and 31, the prior art of record fails to discloses or suggest, individually or in combination the apparatus and method as per claims 10, 25, and 27, wherein "the at least one dual-edged data strobe is gated off from at least a portion of

the at least one processing circuit when the at least one dual-edged data strobe is in high impedance state".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

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